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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known			
		Application Number	10/674,085		
		Filing Date	September 29, 2003		
		First Named Inventor	Elias Fallon et al.		
		Group Art Unit	Not Yet Assigned 2825		
		Examiner Name	Not Yet Assigned Helen		
Sheet	1	of	3	Attorney Docket Number	2879-030564

Rossoshek

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ²			
HR	1	6,161,078		Ganley	12/12/2000	_____
HR	2	6,282,694		Cheng et al.	08/28/2001	_____
HR	3	6,550,046	B1	Balasa et al.	04/15/2003	_____

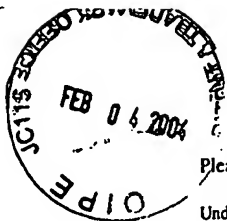
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HR	4	FLORIN BALASA and KOEN LAMPAERT, "Module Placement For Analog Layout Using The Sequence-Pair Representation", Proc. ACM/IEEE Design Automation, pp. 274-279, (June 1999).	
	5	FLORIN BALASA and KOEN LAMPAERT, "Symmetry Within The Sequence-Pair Representation In The Context Of Placement For Analog Design", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 19, No. 7, pp. 721-731 (July 2000).	
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Examiner Signature	/Helen Rossoshek/	Date Considered	05/04/2006
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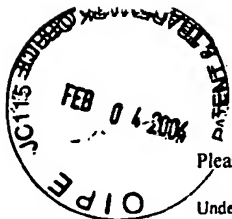
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HR	14	MARGHERITA PILLAN and DONATELLA SCIUTO, "Constraint Generation And Placement For Automatic Layout Design Of Analog Integrated Circuits", pp. 355-358.	
	15	YINGXIN PANG, FLORIN BALASA, KOEN LAMPAERT and CHUNG-KUAN CHENG, "Block Placement Symmetry Constraints Based On The O-Tree Non-Slicing Representation", Proc. ACM/IEEE Design Automation Conference, pp. 464-467, (June 2000).	
	16	JUAN A. PRIETO, JOSE M. QUINTANA, ADORACION RUEDA and JOSE L. HUERTAS, "An Algorithm For The Place-And-Route Problem In The Layout Of Analog Circuits", Pro. IEEE ISCAS, pp. 491-494 (1994).	
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	18	JOHN M. COHN, DAVID J. GARROD, ROB A. RUTENBAR and L. RICHARD CARLEY, "KOAN/ANAGRAM II: New Tools For Device-Level Analog Placement And Routing," IEEE Journal Of Solid-State Circuits, Vol. 26, No. 3, pp. 330-342, (March 1991).	
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	22	HIROSHI MURATA, KUNIHIRO FUJIYOSHI, SHIGETOSHI NAKATAKE and YOJI KAJITANI, "VLSI Module Placement Based On Rectangle-Packing By The Sequence-Pair", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 15, No. 12, pp. 1518-1524, (December 1996).	
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HR	24	R. OKUDA, T. SATO, H. ONODERA and K. TAMARU, "An Efficient Algorithm For Layout Compaction Problem With Symmetry Constraints", In Proc. IBBB ICCAD, pp. 148-151, (November 1989).	

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